

A 3.2 Million Pixel Full-Frame True 2f CCD Image Sensor Incorporating Transparent Gate Technology

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ABSTRACT

This paper describes the performance of an advanced high resolution full-frame architecture CCD imaging device for use in scientific, medical and other high performance monochromatic digital still imaging applications. Of particular interest is the replacement of the polysilicon 2nd gate electrode with that of a more spectrally transparent material thereby dramatically improving device sensitivity. This has been achieved without compromising performance in other areas such as dark current, noise, transfer efficiency and, most importantly, yield.

Keywords: CCD, Image Sensor, Transparent Gate, Full-Frame

1. INTRODUCTION

A great many high-end imaging applications today utilize large format full-frame and frame-transfer style CCD image sensors. The benefits of this architecture are the high sensitivity, high charge capacity and low dark currents resulting in very large dynamic ranges. Because of the relative simplistic nature of the design, very large format sensors have been manufactured at reasonable cost. Typical devices in this class are front-side illuminated and tend to have lower sensitivity (or quantum efficiency—QE) for wavelengths less than 500 nm. The major contributor to sensitivity loss is the overlying polysilicon gate electrode structures, which tend to absorb or reflect incident light depending on wavelength. To circumvent this problem, backside illuminated, UV-sensitive phosphor overlay and virtual phase technologies, among others, have been developed.¹

Backside thinning processes circumvent the polysilicon gates by sensing light from the back of the silicon substrate. In this case, the thick (~500-600 μm) silicon substrates are first reduced to a thickness of ~10 μm in order for the electric fields to 'pull' higher energy (shorter wavelength) induced electrons into the buried channel collection regions. The resulting QE can approach unity for some wavelengths. Thinning processes, however, are very complex and tend to limit themselves to very high performance, low volume applications. UV-sensitive phosphors are special coatings deposited onto the device's surface. These coatings absorb photons in the 200-450 nm range and emit photons at ~550 nm. Above 450 nm, the coatings become transparent. The QE improvement historically has been limited to ~10-15% and the coatings tend to degrade uniformity, cosmetic quality, and to some extent MTF (especially as the pixel size decreases). Virtual or open pinned phase technology replaces polysilicon gates with an open 'phase' where additional ion implantation steps are required to create proper pixel isolation. Here the advantage is that the open phase has less optical restrictions into the substrate—much like the backside system. The drawbacks of this technology in the past have included higher clock swings, charge transfer inefficiency and noise.

An alternative approach is to replace the second level of polysilicon gate electrodes with a more optically transparent conducting gate material made of indium-tin-oxide or ITO.^{2,3} This processing technology has enabled significant improvements in shorter wavelength QE while maintaining the simplicity and high yield (low cost) of front illuminated CCDs. It enables an intermediate cost versus performance choice between current front and back illuminated designs. This technology is applicable to all Kodak full-frame sensors including the *Kodak Digital Science*TM KAF-3200E 2184 x 1472 image sensor, which serves as the basis for this paper. A description of the architecture is given followed by performance measurements made to date.

2. ARCHITECTURE

The KAF-3200E sensor devices are built using heavily doped p-type substrates with a more lightly doped p-type epitaxial layer on top. N-channel transistors and shift registers are built using a single level of doped polysilicon and a single level of ITO gate electrodes. A single level of aluminum connects the gates to bonding pads. Buried channel vertical CCD shift registers are formed, which serves as both the integrating photoactive region and for parallel (line by line) readout of the pixels. A horizontal register accepts each line from the vertical register, one at a time, and shifts pixels to a single output node in a serial fashion. The output node converts the electrons into a voltage, which can be processed and digitized. The total device area measures 16.5 x 11.4 mm and is housed in a 24-pin DIL ceramic package. A general architecture drawing of the device is shown in Fig. 1.

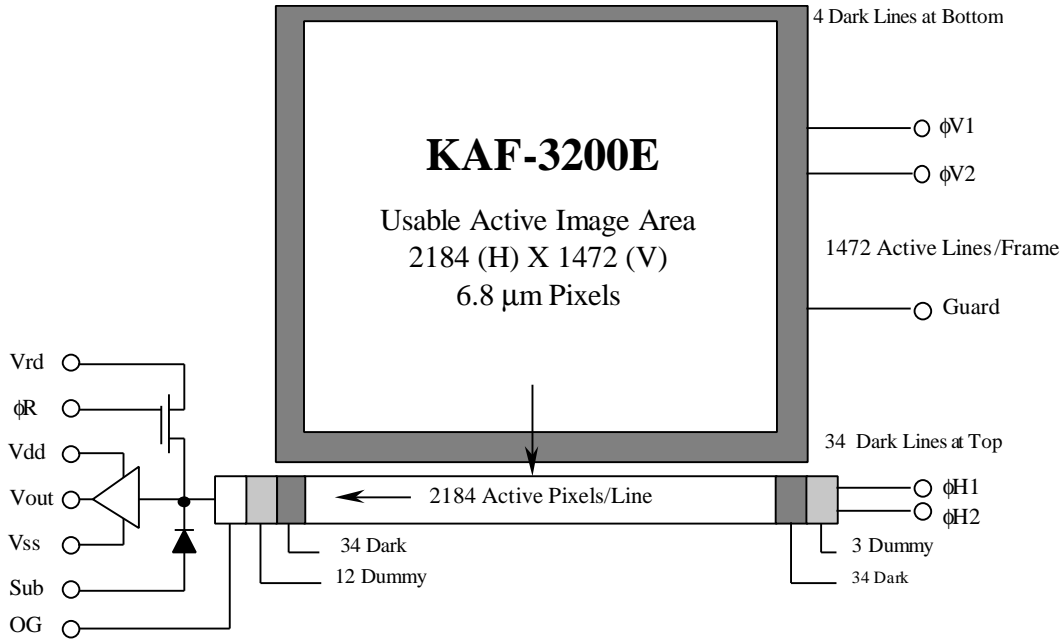


Figure 1. KAF-3200E sensor function diagram.

2.1 Pixel Architecture

The pixel design of the KAF-3200E image sensor employs a true 2 ϕ architecture⁴ and a simplified schematic of the layout is shown in Fig. 2. It is 6.8 μm on a side and contains two gates per pixel, which are called $\phi 1$ (made from polysilicon) and $\phi 2$ (ITO). The ITO material has simply replaced the area previous occupied by a second level of polysilicon. Horizontal running barrier regions are implanted under a portion of each gate, which enables proper vertical isolation of pixels during integration and readout. A field or channel stop region runs vertically that ensures horizontal isolation. 100% of the pixel is photoactive. There are 2184 x 1472 photoactive pixels in each frame. Additional dark reference rows and columns are added along each edge as shown in Fig. 1.

The true 2 ϕ architecture is a highly manufactureable process from a yield perspective. Because each level of conductor ($\phi 1$ and $\phi 2$) is driven with the same clock, intra-level shorts are not fatal—rather cosmetic defects are created, which can be still acceptable depending on the application and cost requirements. A $\phi 1$ to $\phi 1$ short is likely to cause column defects while $\phi 2$ to $\phi 2$ shorts appear more like a point or cluster defect. As pixel sizes shrink, the true 2 ϕ process provides less demanding requirements on photolithography than 3 or 4 phase devices. One drawback to the architecture lies in the fixed channel potential difference between barrier and storage regions within a pixel. The process essentially fixes this capacity and clocking levels will have little effect of increasing or decreasing this amount.

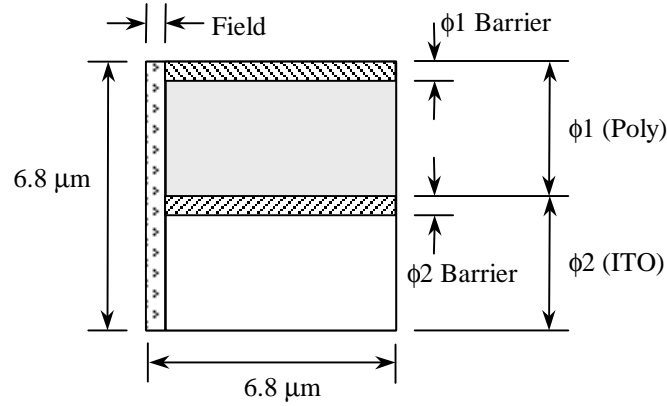


Figure 2. KAF-3200E sensor pixel architecture.

2.2 Shift Register Operation

During integration, both phases are held in accumulation with a negative voltage as represented in Fig. 3a. Following integration, charge from both phases are recombined into $\phi 2$ by applying a positive voltage on $\phi 2$ (3b). The voltage polarities of $\phi 1$ and $\phi 2$ are reversed to transfer charge from $\phi 2$ to $\phi 1$ (3c). Switching the voltages of both phases again push charge from $\phi 1$ to $\phi 2$ of the next pixel (3d). The cycle completes when $\phi 2$ returns to accumulation with a negative voltage (3e). At this point a line of charge has been presented to the horizontal register that transfers charge in traditional complementary clocking to the output. This method of clocking is commonly referred to as MPP⁵ or accumulation mode and was first introduced by Saks.⁶ By maximizing the amount of time the gates are held with a negative voltage, the dark current generation rate is greatly reduced. The negative voltage on the gates causes holes to accumulate near the oxide/silicon surface. These holes neutralize (recombine) unwanted electrons which are emanating from this interface leaving only the depletion and bulk components of device dark current.

Unlike many designs, the true 2 ϕ architecture of this device is able to implement MPP mode without degradation of charge capacity. It works by building in an offset difference in the barrier potentials of each phase relative to one another while in the accumulated state. During the last cycle of MPP mode (Fig. 3e) the charge capacity under $\phi 2$ begins to collapse. Because the barrier potential under $\phi 2$ is slightly deeper than $\phi 1$, excess charge is always preferentially spilled backwards into the adjacent $\phi 1$ thereby increasing overall pixel capacity.

2.3 Optical Injection Test Pixels

Traditional methods of monitoring horizontal charge transfer efficiency (CTE) have included electrical injection input structures and X-ray radiation sources. The difficulty with electrical injection structures (additional gates and diodes added at the end of a CCD shift register where charge packets are created by ‘clocking’ an impulse into the array) is that they require adjustment for each individual die thus making automation more difficult. X-ray radiation sources, such as Fe⁵⁵, provide a known and constant input level but the additional apparatus and safety precautions inhibit its use in a production test environment. The fixed energy levels of a particular isotope also prohibit the ability of measuring CTE as a function of signal level.

Contained within the ‘Dummy’ pixels from Figure 1 are special pixels that enable in-situ monitoring of CTE. It consists of a photoactive column at the leading and trailing edge of the device beyond the dark reference regions. In order to remove optical and diffusion crosstalk components, scavenging columns are added that transfer charge in the opposite direction of normal vertical charge transfer. Drains are provided at the top of the array to remove any charge collected in these pixels. The input stimulus is supplied by simply illuminating the sensor with light. Varying light intensity or exposure produces a transfer curve comparing transfer efficiency as a function of signal. The resulting horizontal profile can be used to calculate the transfer efficiency in the case of few transfers (leading edge) and many transfers (trailing edge). See Figure 4.

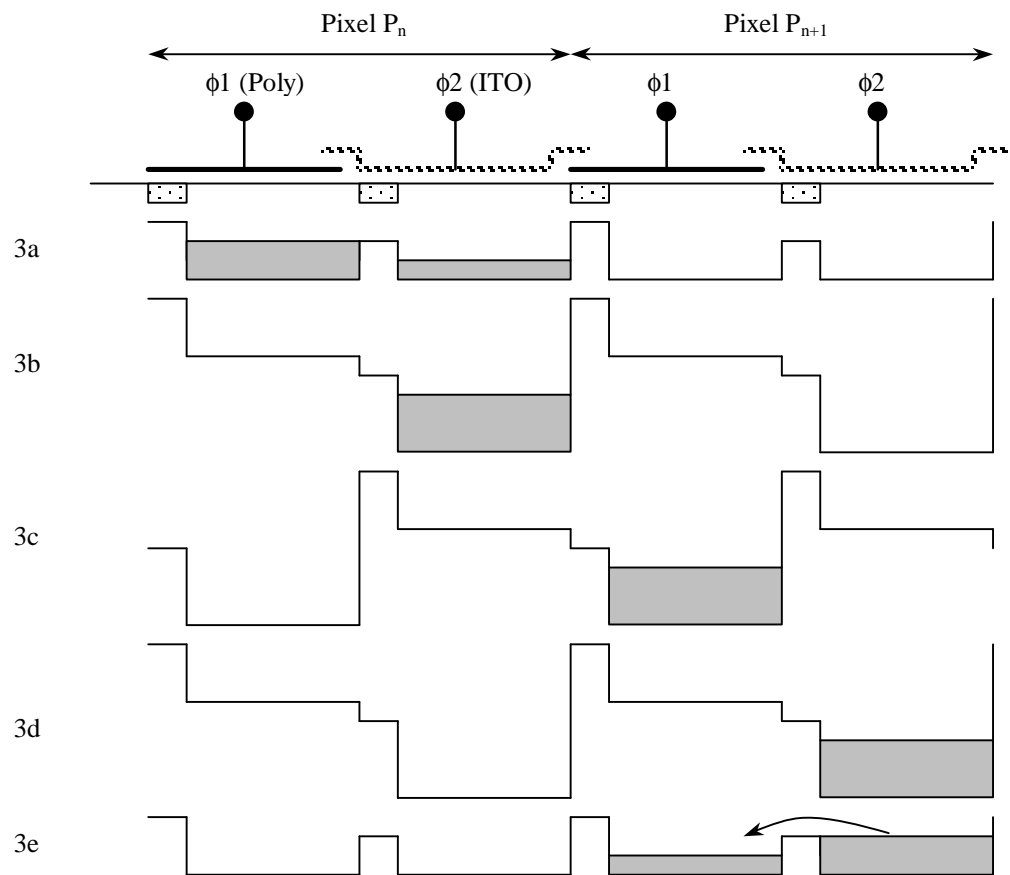


Figure 3. Vertical shift register operation.

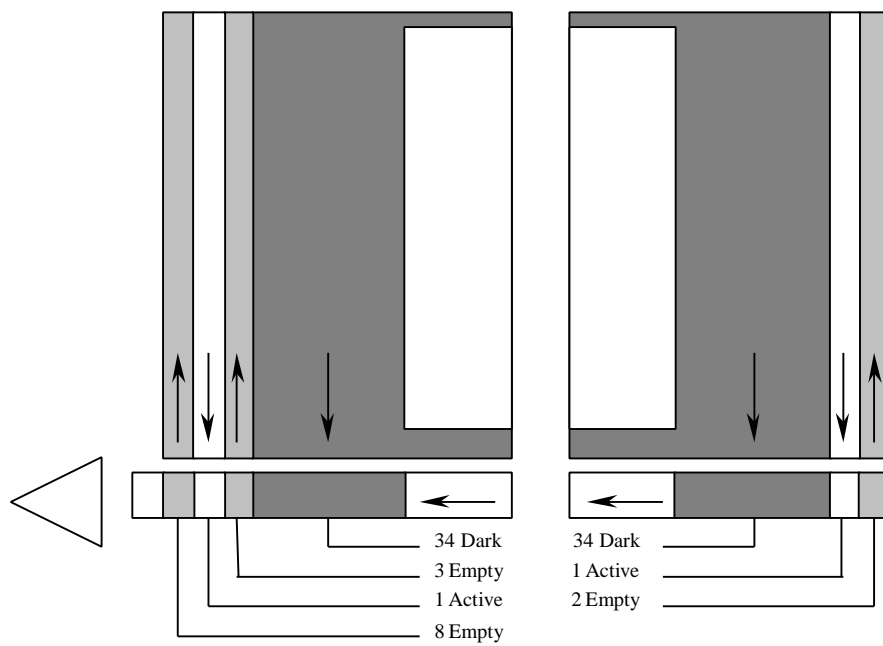


Figure 4. Optical Injection Test Pixels.

2.4 Design Summary

Attribute	Value	Units
Total Chip Size (H x V)	16.5 x 11.4	mm ²
Photoactive Area (H x V)	14.85 x 10.01	mm ²
Pixel Size (H x V)	6.8 x 6.8	μm ²
Total Photoactive Pixels	2184 x 1472	#
Fill Factor	100	%
Outputs	1	#
Clocks	5	#
DC Supplies (excluding Gnd)	5	#

Table 1. KAF-3200E Design Summary

3. PERFORMANCE

In the following sections, key performance metrics are evaluated and compared between traditional double level polysilicon and ITO second gate-based processes where appropriate. These include the quantum efficiency, dark current and linearity. Other performance parameters have been confirmed not to vary with process/design differences.

3.1 Quantum Efficiency Measurements

Quantum Efficiency (QE) or spectral response is the number of electron-hole pairs (e-) created and successfully readout of the device for each incoming photon. It is represented as a percent or in terms of e-/photon. In simple silicon based imaging, it can never exceed 100% efficiency.

The QE of the ITO and polysilicon devices are measured as a function of wavelength from 350 to 1100 nm. Current equipment capability prevents measuring below 370 nm at this time. In Fig. 5, the QE of the KAF-3200E sensor (6.8 μm pixel ITO process) is compared to that of the KAF-1400 sensor (6.8 μm double poly process). The ITO process, due to it's better transmission properties, is clearly superior at wavelengths less than ~750 nm with an improvement exceeding 10x at 400 nm (from 2.6% to 28%). At wavelengths above ~750 nm, there is little difference in the designs because the polysilicon and ITO materials have similar transmission characteristics. As wavelengths approach 1100 nm, photons are being absorbed much deeper into the silicon where there are less electric fields available to collect the signal. At the theoretical limit of ~1100 nm the photons appear transparent to silicon.

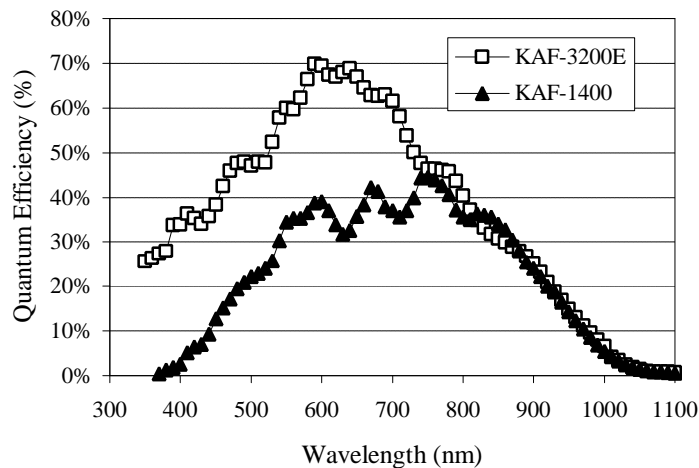


Figure 5. KAF-3200E (6.8μm pixel Poly/ITO Process) vs KAF-1400 (6.8μm pixel Poly/Poly Process) Quantum Efficiency.

3.2 Dark Current Measurements

The dark current in a device represents an offset in the signal level measured in the absence of any light. It is typically specified as an average value for all pixels. The average dark current, however, is rarely a concern in an imaging system because this value can be easily removed either in the analog or digital domain. The exception to this is if the level is so high that the loss in effective charge capacity drops below required levels. Instead, it is the variability of the dark current in each pixel that degrades image quality. Dark current noise will degrade image quality by either (1) a fixed pattern non-uniformity from pixel to pixel or (2) as a shot noise component where the value in each pixel varies from frame to frame depending on the level of the average dark current level of that pixel. Dark current will vary strongly depending on temperature level. As the temperature increases, the energy of electrons in the valence band increases, thereby improving chances of a transition into the conduction band where it becomes free to be collected and sensed by the device.

The dark current has been measured at several temperatures for the KAF-3200E device. The dark current generation rates between the polysilicon and ITO processes are essentially the same within the tolerance of lot to lot variations. At room temperature, the typical dark current has been measured to be $< 10 \text{ pA/cm}^2$. The dark current has been found to double for every 6°C increase in temperature.

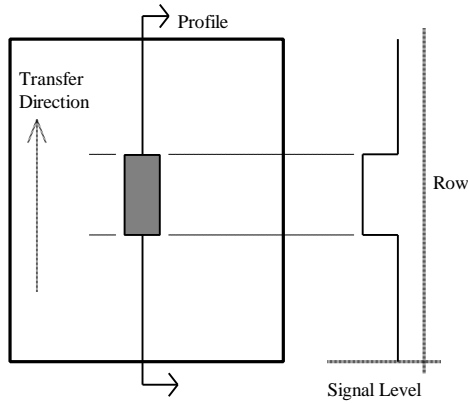
3.2 Photon Transfer Measurements and the Delayed Exposure Test Method

Imaging with a CCD device is an inherently linear process. It is primarily limited by the linearity of the output amplifier and the charge transfer efficiency (which commonly exceeds 99.9995% efficiency per gate transfer depending on frequency on and signal level). This provides very precise measurements of light quanta—both in signal intensity level and geometric arrangement. Janesick, et al. have devised an absolute method to measure or calibrate a CCD for linearity in addition to providing values for system noise, charge-voltage conversion gain, and full-well charge capacity. This method is called the Photon Transfer Technique.⁷ It utilizes the fact that the amount of rms noise associated with an exposure level of photons is exactly equal to the square root of the average value provided sufficient sample points are available.

The measurement technique used for the ensuing performance parameters was generated with a modified approach to the Photon Transfer method. Rather than capturing multiple frames to determine each data point in the curve, the entire curve can be constructed with only one or two captures using a delayed exposure technique. Referring to Fig. 6, the principle is to expose the device while the vertical shift register has already begun shifting charge to the output—similar to time delay and integration (TDI) imaging. As lines are clocked out of the device (or under the light shielded rows), they no longer receive additional exposure. The first line out will have one line time of exposure, the second will have two and so forth. A convenient illumination source for this test is LEDs where the light can be precisely gated and synchronized to line times. The resulting vertically ‘smeared’ image contains a linear ramp (both up and down in signal levels), which can then be analyzed for photon statistics on a line-by-line basis. In practice, it is difficult to precisely focus object edges on the device to know where the ramp begins or ends. By using dark reference rows (either leading or trailing) built into the device with a flat field exposure enables a more controlled and production test worthy feature. Typically, the trailing edge is used that will fold vertical transfer inefficiency effects into the ramp data. Using the trailing edge also requires the system to clock and capture additional lines through the array than would normally be done. The number of data points in the curve is determined by the number of line times the exposure is overlapped into the readout. By increasing or decreasing light intensity levels (again LEDs make this convenient), the resolution between data points can be made coarse or fine - even down to the electron per point levels. Aside from significant reduction in measurement times, this method also reduces errors caused by low frequency drifts in electronics or exposure conditions.

3.3.1 Charge Capacity and Low Level Non-Linearity

The charge capacity is evaluated by determining the point along the linearity curve (signal vs exposure), which deviates by a pre-determined percentage (typically 1%) from a straight line. The straight line is determined as the least squares linear fit to the central values of the curve. Using only the center values allows each end to ‘float’ thereby highlighting problems at the high or low end of the signal range. The 1% linear saturation voltage of the KAF-3200E shown in Fig. 7 measures $\sim 1300 \text{ mV}$.



*Note: The dark rectangle represents a focused object on the CCD.

Figure 6a. Standard exposure and readout.

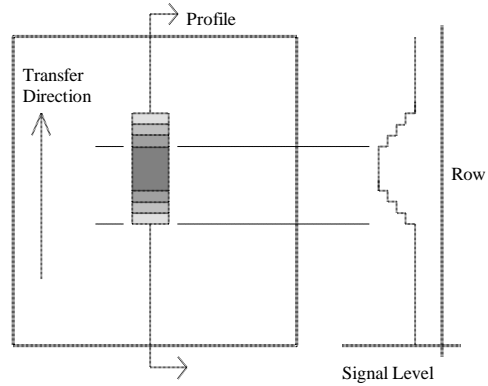


Figure 6b. Delayed exposure timing.

The low signal level non-linearity is defined as the Y-axis intercept (Yint) from the straight line fit as described in the preceding paragraph. It is measured in units of DN or mV. As linearity degrades, the value of Yint deviates from 0. Percentages are avoided at the low end where signal levels are very small and measurement noise begins to dominate. The Yint of the KAF-3200E sensor device shown in Fig. 7 has been measured to be +8.9 mV when using the central ¼ points for the least squares fit of the linearity curve.

3.3.2 Charge to Voltage Conversion Gain

Referring again to Janesick,⁷ et al., the conversion gain is determined from the slope of the mean signal level versus the variance using digital counts (DN) from the analog to digital converter. Instead of determining these values from a subsection within the array, the measurements come from single lines within the delayed exposure ramp. The inverse slope represents the conversion gain in units of e-/DN. Knowing the system gain (V/DN) provides units of V/e-. For the KAF-3200E sensor device shown in Fig. 8, this results in 18.9 $\mu\text{V}/\text{e-}$.

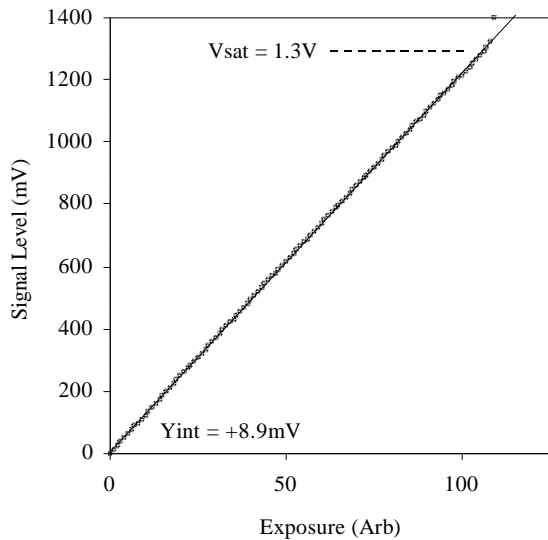


Figure 7. Signal vs exposure using delayed exposure method.

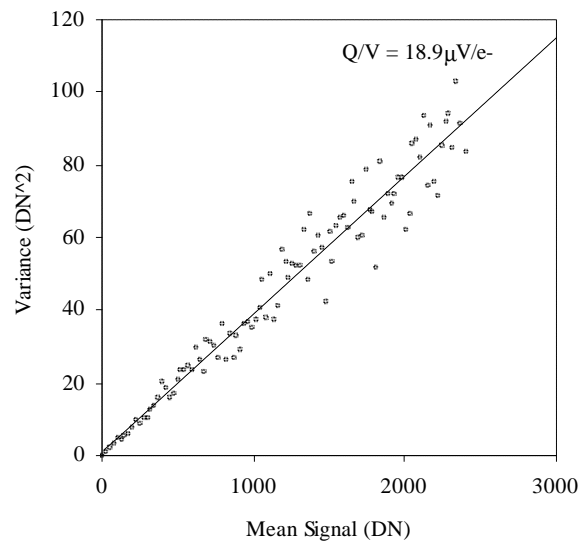


Figure 8. Mean-variance plot to determine Charge-to-voltage conversion.

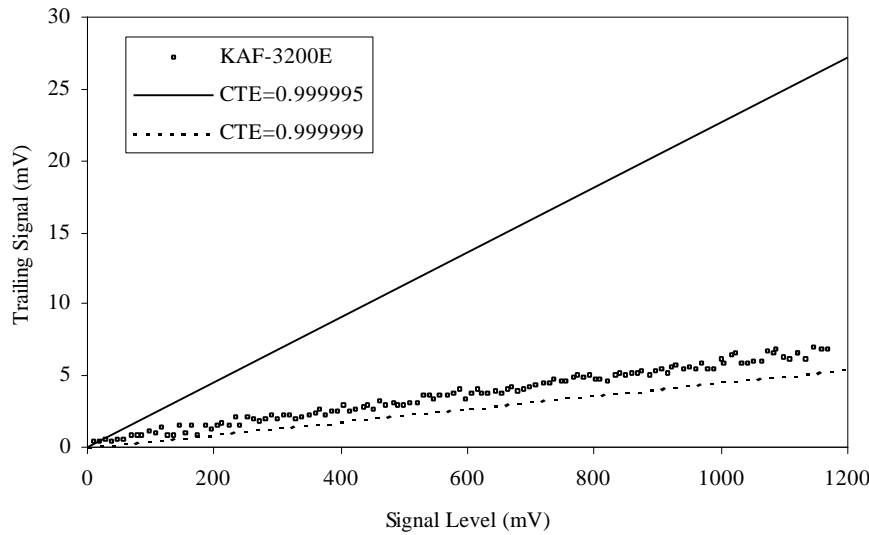
3.3.3 Noise and Dynamic Range

The noise in a CCD tends to be dominated by the on-chip amplifier. Because the transistors of the KAF-3200E devices are all made using the first level of polysilicon, we expect the noise to be independent of the ITO or double polysilicon processes. As the mean signal level decreases in the photon transfer curve, the readout noise of the sensor and electronics dominate. The lowest noise value acquired represents the total noise. To obtain the sensor noise, the CCD's output is disconnected to the signal processing, which yields the electronic noise caused by the system. This total value is discounted by the system noise (in quadrature) and the KAF-3200E sensor yields a sensor noise of $\sim 10\text{e}^-$ rms.

The dynamic range is defined as the charge capacity divided by the sensor noise. For this KAF-3200E device this amounts to 77 dB or 12.8 bits.

3.4 Charge Transfer Efficiency Measurements and the Delayed Exposure Test Method

Using the same delayed exposure image capture described in section 3.3, the charge transfer efficiency in the horizontal direction can be derived as a function of signal level at a test frequency of 4 MHz. This is achieved using the optical injection test feature that was described in 2.3. Fig. 9 below plots the illuminated signal value of the light sensitive column at the end of the horizontal CCD (opposite the output amplifier) as a function of the signal found in the adjacent (trailing) column. Knowing the number of transfers enables a calculation of the charge transfer efficiency.



4. SUMMARY

A 3.2 million pixel CCD imaging device has been developed using ITO transparent gate technology. This technology significantly improves quantum efficiency at wavelengths below 750 nm, while maintaining similar performance between 750 and 1100 nm. This has been achieved without adding additional complexity to the manufacturing process or degrading other performance aspects of the device compared to the traditional double polysilicon process. These devices join a family of full-frame devices now being produced using this technology (see Table 2).

Sensor Device	Pixels (H x V)	Pixels (Mpixels)	Pixel Size	Antiblooming Protection
KAF-0261E	512 x 512	0.26	20 μm	No
KAF-0401E	768 x 512	0.4	9 μm	No
KAF-0401LE	768 x 512	0.4	9 μm	Yes
KAF-1001E	1024 x 1024	1.0	24 μm	No
KAF-1301LE	1280 x 1024	1.3	16 μm	Yes
KAF-1401E	1320 x 1035	1.4	6.8 μm	No
KAF-1602E	1536 x 1024	1.6	9 μm	No
KAF-1602LE	1536 x 1024	1.6	9 μm	Yes
KAF-3200E	2184 x 1472	3.2	6.8 μm	No
KAF-6303E	3072 x 2048	6.3	9 μm	No
KAF-6303LE	3072 x 2048	6.3	9 μm	Yes

Table 2. Current Full-Frame CCDs from Kodak employing ITO transparent gate technology.

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